Polylithic Integration of 2.5D and 3D Chiplets Using Interconnect Stitching

Paul K. Jo, Ting Zheng, and Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA 30318, USA
mbakir@ece.gatech.edu

***Abstract*— This paper explores polylithic integration of heterogeneous dice (chiplets) for high-density electronic systems. In this approach, stitch-chips are used to enable 2.5D integration by providing dense signal pathways between assembled 'anchor chips,' while surface-embedded chips provide 3D face-to-face electrical interconnection with corresponding anchor chips. Multi-height Compressible MicroInterconnects (CMIs) are used to enable low-loss and mechanically robust interfaces between the anchor chips and the stitch-chips as well as the surface-embedded chips. Fabrication and assembly of a testbed is reported and demonstrates robust interconnection. In an effort to characterize the CMIs and stitch-chip channels at high-frequency, electromagnetic simulations are carried out and demonstrate less than 0.6 dB insertion loss for 90 µm tall CMIs and 500 µm long channels on a fused silica stitch-chip.**

Keywords-Compliant interconnects, 2.5D and 3D ICs, heterogeneous integration

I. INTRODUCTION

In the era of ubiquitous computing, Internet-of-Things (IoT), Artificial Intelligence (AI), 5G, self-driving vehicles, and big data, the number of connected electronic devices and volume of data generated are sharply increasing [1], [2]. These have pushed the semiconductor industry towards ever more complex and sophisticated chip designs for better computing capabilities. Over the last several decades, this has been enabled by system-on-chip (SoC) designs in which various functionalities have been integrated into a single die using monolithic processes along with technology scaling [3]. However, Moore's Law is slowing down and approaching its limits while SoC design complexity and fabrication costs continue to increase [4], [5]. These emerging challenges have introduced significant research in high-density multi-die integration technologies by virtue of their integration flexibility, potential reduced fabrication costs, and ability to mix-and-match across different technologies (i.e., chiplet design approach) that include silicon interposer, Embedded Multi-chip Interconnect Bridge (EMIB), and Foveros 3D integration technologies [6], [7]. The benefits of these heterogeneous integration approaches have been show recently. For example, AMD and GLOBALFOUNDRIES have reported approximately 40% and 63% reduction in silicon fabrication cost along with improved system-level performance through 2.5D and 3D integration, respectively [8], [9].

In this paper, we extend our prior work [10] to demonstrate a polylithic integration technology of heterogeneous dice to enable *the ultimate flexibility* in 2.5D/3D multi-die chiplet integration yet providing monolithic-like performance and low-loss dense signal interconnections. Fig. 1 illustrates a schematic of the proposed integration technology. Firstly, multiple 'anchor chips' are concatenated by 'stitch-chips' with dense interconnects, which are placed between the anchor chips and the package substrate. If needed, 'surface-embedded chips,' which may be passive or active dice, can be integrated underneath the anchor chips. Vertically flexible off-chip interconnects, which we call Compressible MicroInterconnects (CMIs) [11], are used to provide signal interconnections between the assembled dice. CMIs on the edge of the anchor chips are fine-pitch to provide high bandwidth interconnection between the anchor chips through the stitch-chips [10]. Multi-height CMIs are used to enable interconnections between the anchor chips and the surface-embedded chips. Power delivery and signal interconnections from the package substrate can also be enabled by the multi-height CMIs. Mechanical bonding between the anchor chips and the package substrate is enabled by using large solder bumps on each of the four die corners to enable reworkability of the assembled die. The stitch-chips, in the simplest form, provide high-bandwidth density signal pathways between the anchor chips, yet they can include high-quality passives

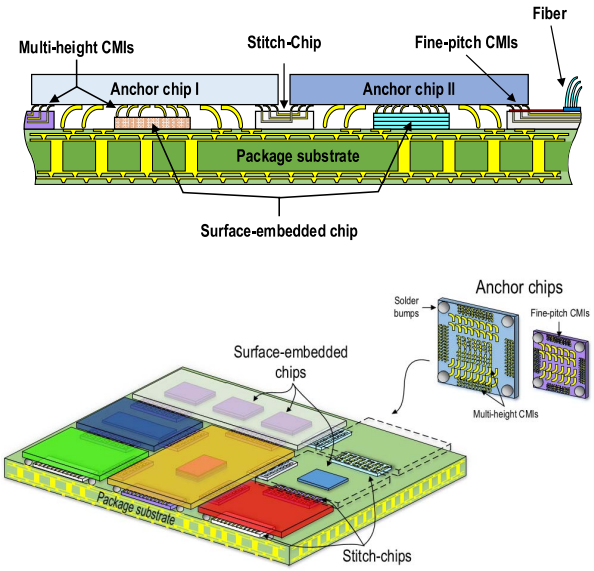

Fig. 1. Schematic of polylithic integration for heterogeneous dice using multi-height CMIs

2377-5726/19/$31.00 ©2019 IEEE
DOI 10.1109/ECTC.2019.00278

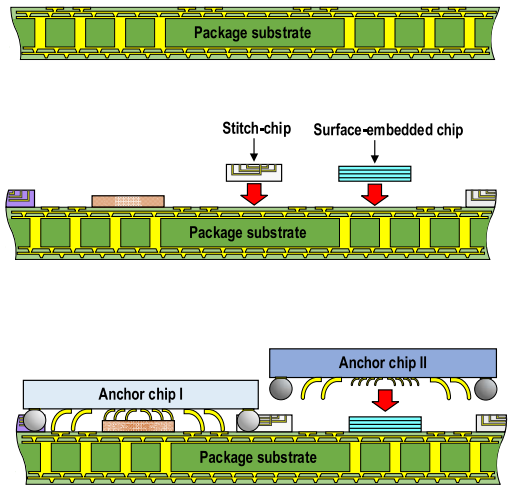

Fig. 2. The assembly process flow

and/or active circuits as well. This approach can also enable direct interconnection between the anchor chip and a silicon photonic integrated circuit (PIC) with direct fiber assembly, as illustrated in Fig. 1. The anchor chips may be an ASIC, CPU, GPU, FPGA, MMIC, or photonic die, and the surface-embedded chips may be memory dice, power conversion chips, or Integrated Passive Device (IPD) dice, for example.

Since the CMIs are elastically compressible unlike conventional solder bumps, the proposed polylithic integration technology can compensate for any possible off-chip interconnection distance differences resulting from chip thickness differences; this enables both 2.5D and 3D face-to-face interconnection in one platform, as shown in Fig. 1. In addition, CMIs can provide temporary interconnection, which can improve package and system yield as CMIs facilitate die replacement/rework. The mechanical compliance of the CMIs can also improve the thermomechanical reliability of the assembled system [12] as well as enabling flexibility in dice and substrates to be stitched together irrespective of CTE mismatch (e.g., silicon, glass, organic, and GaN).

This paper is organized as follows: Section II describes the fabrication and assembly process of the proposed integration technology. In Section III, HFSS simulations of stitch-chip links are demonstrated. Finally, in Section IV, concluding remarks are stated.

II. Fabrication and Assembly of Stitch-Chip Based Polylithic Integration

Fig. 2 shows the overall assembly process flow of the proposed polylithic integration technology. The integration process begins with forming traces and pads on the package substrate. Next, the stitch-chips and/or surface-embedded chips are attached onto the package substrate. The anchor chips with multi-height CMIs and relatively large solder bumps are flip-chip bonded onto the package substrate, as shown in Fig. 2 (note, CMIs can be on the stitch-chips instead). Finally, the assembly is completed by reflowing the solder bumps. NiW is used to form the core of the CMIs due

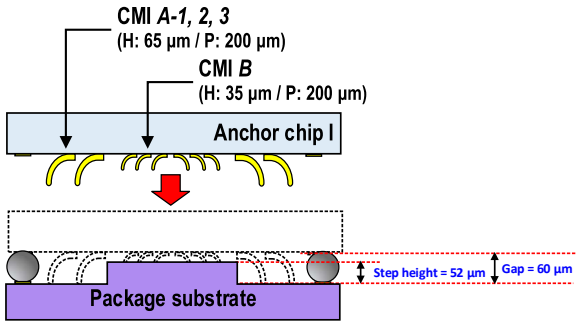

Fig. 3. Schematic of the fabricated testbed

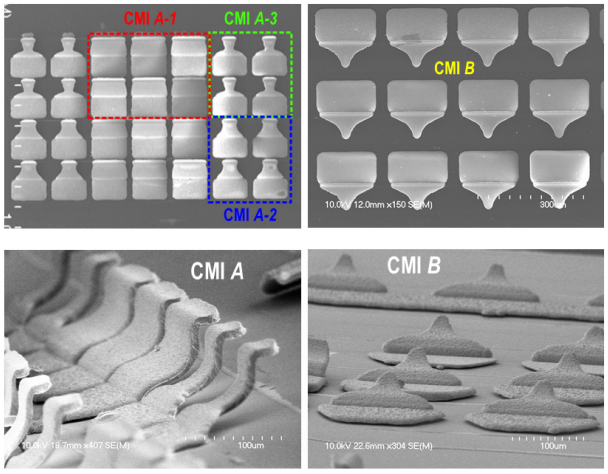

Fig. 4. SEM images of the fabricated multi-height CMIs

to its high yield strength of 1.93 GPa [11]. This high yield strength enables the CMI to tolerate larger stress before experiencing plastic deformation during compression. The NiW CMIs are electroless gold plated as the final fabrication step to prevent oxidation.

The testbed is fabricated and assembled in order to demonstrate the key features of the proposed technology: assembly of an anchor chip with multi-height CMIs onto a substrate with a surface-embedded chip and mechanical bonding using solder bumps. In the testbed, the surface-embedded chip on the package substrate is emulated by forming a tall step on the silicon substrate. Four solder bumps are also fabricated on the silicon substrate to mechanically secure the assembled testbed. For the anchor chip with multi-height CMIs, two CMI designs with different heights, which we refer to as CMI *A* and CMI *B* in this paper, are fabricated on a silicon substrate. Both CMI *A* and *B* designs are formed on a 200 µm pitch while the heights are different. Specifically, for CMI *A*, three different CMI designs (*A-1*, *A-2*, and *A-3*) of the same height are designed to demonstrate the simplicity of CMI compliance engineering. Fig. 3 shows a schematic of the fabricated testbed. Note, in prior work, we demonstrated the fabrication of CMIs with 20 µm of in-line pitch [10].

SEM images of the fabricated anchor chip are shown in Fig. 4. An approximately tapered design is used for the

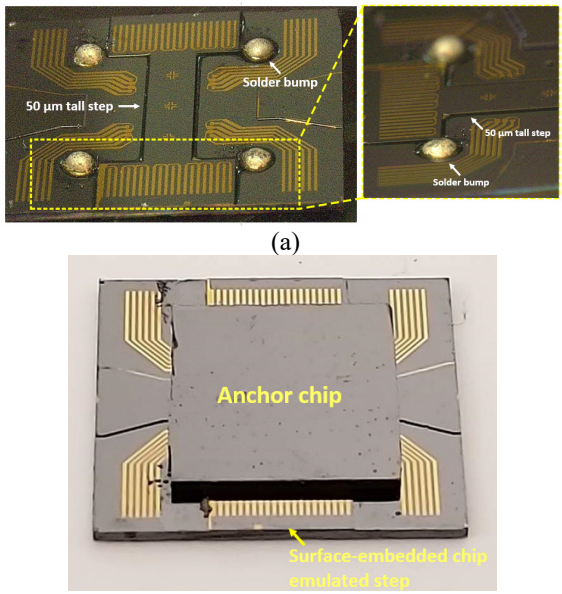

Fig. 5. Optical images of the testbed: (a) the silicon substrate with the step and solder bumps and (b) the assembled testbed

different CMI designs in order to distribute the stress along their length during deformation. The upward-curved cross-sectional design ensures that the tip of the CMI maintains contact with the corresponding pad during assembly. Both fabricated CMI *A* and *B* have 200 µm pitch while the heights are approximately 65 µm and 35 µm, respectively.

Fig. 5 shows optical images of the fabricated silicon substrate with emulated surface-embedded chips (and solder bumps) and the assembled testbed. In this testbed, the step height is approximately 52 µm. Spherical solder balls with a diameter of 500 µm are manually attached and reflowed on the metal pads before assembly (though electroplating can be used to fabricate the solder bumps as well). Thermocompression bonding is used to assemble the dice. Once the anchor chip is aligned to the substrate, the solder balls are reflowed again to provide mechanical interconnection between the anchor chip and the substrate while maintaining approximately 60 µm of gap.

Mechanical compliance, a key property of CMIs, was measured using a Hysistron Triboindenter. The measured average compliance was 2.42 mm/N, 3.86 mm/N, 6.1 mm/N, and 5.4 mm/N, respectively for CMI *A-1*, CMI *A-2*, CMI *A-3*, and CMI *B* designs. These results illustrate the simplicity of CMI mechanical compliance engineering through only photomask geometry re-design (though there are additional parameters that impact compliance including thickness, material, and three-dimensional curved geometry). The four-point resistances of the interconnections after assembly were measured using a Karl-Suss probe station. The four-point resistance values of CMI *A-1* and CMI *B* were measured, and their average four-point resistance, including contact resistance with the gold pads, is 190.8 mΩ and 64.4 mΩ, respectively. We believe the contact resistance between the

TABLE I
DIMENSIONS AND MECHANICAL AND ELECTRICAL CHARACTERIZATION RESULTS OF THE FABRICATED MULTI-HEIGHT CMIS

Interconnect	Pitch (µm)	Height (µm)	Compliance (out-of-plane) (mm /N)	Four-point resistance (mΩ)
CMI *A-1*	200	65	2.42	190.8
CMI *A-2*			3.86	-
CMI *A-3*			6.1	-
CMI-*B*	200	35	5.4	64.4

CMIs and the pads contributes to this difference in the average resistances; as shown in Fig. 3, the 60 µm gap (between the silicon substrate and the anchor chip) deforms the 65 µm tall CMI *A* by approximately 5 µm while the 8 µm gap (between the step and the anchor chip) deforms the 35 µm tall CMI *B* by approximately 27 µm; this will affect the contact force and hence contact resistance of the CMIs. Table I summarizes the compliance and four-point resistance characterization results and the dimensions of the fabricated multi-height CMIs.

III. STITCH-CHIP LINK SIMULATION

In order to characterize the high-frequency properties of the multi-height CMIs and the stitch-chip links both in aggregate form and individually, a carefully constructed testbed must be designed, fabricated, and experimentally tested to validate the models. In this paper, we present the initial design and simulation results of such a testbed. Since the L-2L de-embedding method has been widely utilized for the characterization of transmission lines with through silicon via (TSV) in the RF range [13], [14], our stitch-chip based high-frequency testbed is designed to be compatible with L-2L de-embedding.

Fig. 6 shows the details of our ANSYS HFSS testbed model. The model contains a 2.5D signal link, whose ABCD-matrix is denoted as [2.5D-Link] in Fig. 6 (a). As shown in Fig. 6 (a), this 2.5D channel can be partitioned into a single CPW intermediate channel, two G-S-G pairs of CMIs whose ABCD-matrices are denoted as [CMI] and two extended CPW T-line whose ABCD-matrices are denoted as [TL]. The two extended CPW T-lines can be de-embedded and the remaining structure, as shown in Fig. 6 (b), is called the stitch-chip link whose ABCD-matrix is [Link1′]. In practice, the tip of the CMIs would touch the CPW T-lines and deform elastically.

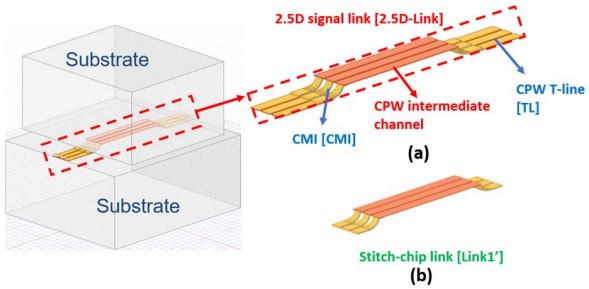

Fig. 6. HFSS model of stitch-chip channel

However, this deformation is not accounted for in this work. L-2L de-embedding requires two 2.5D signal links, one of which has an intermediate channel length twice as long as the other (ABCD-matrices [2.5D-Link1] and [2.5D-Link2]). [2.5D-Link1] and [2.5D-Link2] can be derived from the S-matrices measured from a vector network analyzer. After de-embedding the two extended CPW T-lines, the stitch-chip link's ABCD-matrix can be obtained. The procedure of this L-2L de-embedding can be summarized as follows [13], [14]:

$$[Link1'] = [TL]^{-1}[2.5D - Link1][TL]^{-1} \quad (1)$$

$$[Link2'] = [TL]^{-1}[2.5D - Link2][TL]^{-1} \quad (2)$$

$$[CMI] = \left(\sqrt{[Link1']^{-1}[Link2'][Link1']^{-1}}\right)^{-1} \quad (3)$$

where [Link1′] and [Link2′] represent [2.5D-Link1] and [2.5D-Link2] after de-embedding the CPW T-lines at both ends. It should be noted that [Link1′] represents an ABCD-matrix of a stitch-chip link that consists of a CPW with CMIs on both ends. Thus, based on L-2L de-embedding, our designed testbed can potentially extract the electrical properties of both CMIs and stitch-chip links with high accuracy.

In the simulated testbed, the substrate material used for the stitch-chip is fused silica, which provides relatively low dielectric constant (~3.9) and loss tangent (~0.0002) within the RF range. The low dielectric constant and loss tangent enable low-loss transmission line design. Second, all CPWs are made using copper and their characteristic impedances are optimized to 50 Ω. In Fig. 6, the CPW intermediate channel will have two lengths, one of which is twice the other. The extended CPW T-line is fixed at 250 µm length while the total stitch-chip link has 500 µm-long CPW, as shown in Fig. 6 (b). Lastly, several design versions for the CMIs have been included. Fig. 7 illustrates the cross-sectional view of one nickel-core CMI (thickness varies from 5 µm to 7 µm) coated with 500 nm-thick gold to avoid oxidation and to decrease resistance (DC and AC) [15]. Table II summarizes the key dimensions for different CMI designs. In Table II, AR refers to the aspect ratio of the CMI and is defined as the ratio of the CMI's horizontal length (L) and vertical height (H) (see Fig. 7). Arc length (AL) represents aggregate physical length of the CMI.

Simulations from DC to 30 GHz are conducted utilizing above models. Following conversion of S-matrices to ABCD-matrices and using model (1), an ABCD-matrix and S-matrix of the stitch-chip link (CMI+CPW+CMI) can be extracted. In order to validate the de-embedding method, a standalone case where a stitch-chip link has the same dimensions as the de-embedded stitch-chip link is set up as a reference (REF link). S_{21} and S_{11} for different stitch-chip link designs are shown in Fig. 8. The magnitudes of the insertion loss (S_{21}) and the return loss (S_{11}) of the reference link and the testbed link after de-embedding are compared and show agreement. The stitch-chip links exhibit an insertion loss of less than 0.6 dB within 30 GHz and maintains good impedance matching (return loss better than -10 dB) even with largest CMIs (90 µm-high).

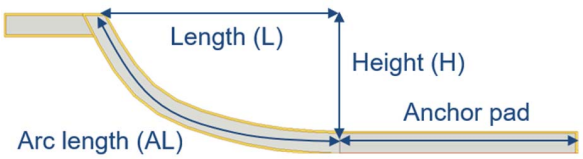

Fig. 7. Cross-section view of CMI with design parameters

TABLE II
DESIGN POINTS FOR DIFFERENT CMI VERSIONS

CMI design	AR = L / H	H (µm)	L (µm)	AL (µm)
60 µm-high CMI	2	60	120	145.3267
90 µm-high CMI	2	90	180	217.9901
90 µm-high CMI	1	90	90	141.3717

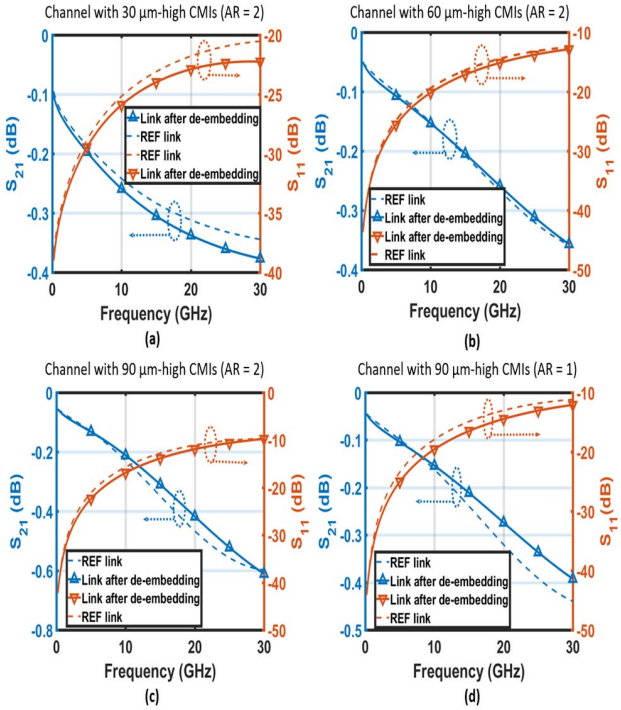

Fig. 8. S-parameters results compared with standalone link (CMI+Tline+CMI). De-embedded link with (a) 30 µm-high CMIs (AR = 2); (b) 60 µm-high CMIs (AR = 2); (c) 90 µm-high CMIs (AR = 2); (d) 90 µm-high CMIs (AR = 1)

Another objective of this testbed is to extract the electrical parasitics of the CMIs. After converting S-matrices to ABCD-matrices and following the models in (1) to (3), an ABCD-matrix and S-matrix of CMIs can be easily extracted. Fig. 9 shows the S_{21} and S_{11} for different CMI designs. As for S_{21}, CMIs provide low-loss 3D interconnect solution within the RF range (insertion loss better than -0.11 dB). For S_{11}, CMIs still maintain acceptable impedance matching thanks to their electrically short structure. Note that by only reducing AR, the

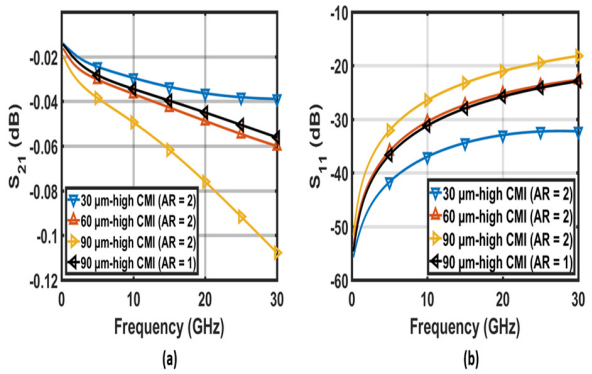

Fig. 9. S-parameters comparison for CMIs with different heights: (a) Insertion loss; (b) Return loss

90 μm-high CMI's loss is improved. The reason is that shrinking AR down from 2 to 1 results in approximately 35% reduction in physical length. Because of their short length relative to wavelength, a lumped model [16] can be used to extract RLGC parasitics. The RLGC parasitics can be extracted using [16]:

$$R = real\left(\frac{-2}{Y_{12}+Y_{21}}\right) \tag{4}$$

$$L = \frac{imag\left(\frac{-2}{Y_{12}+Y_{21}}\right)}{2\pi f} \tag{5}$$

$$G = real\left(2Y_{11} + (Y_{12} + Y_{21})\right) \tag{6}$$

$$C = \frac{imag\left(2Y_{11}+(Y_{12}+Y_{21})\right)}{2\pi f} \tag{7}$$

where f is frequency. Table III summarizes the RLGC parasitics for some of the CMI designs at 30 GHz. Most of the CMI interconnect is surrounded by air, which results in low parasitic capacitance and conductance.

IV. Conclusion

This paper explores the fabrication and assembly process of a stitch-chip based polylithic integration enabled by multi-height CMIs. Experimental characterization of the proposed approach was performed by assembling the testbed using multi-height CMIs and surface-embedded chips emulated using a silicon step. The experimental results show that the multi-height CMIs can enable robust electrical interconnection irrespective of off-chip interconnection distance differences. These results demonstrate a new degree of freedom in system-level integration when compared to conventional solder bumps. In this paper, we also present HFFSS-based simulations of the CMIs and stitch-chips to gain initial insight into their high-frequency response.

Acknowledgment

This work was performed in part at the Georgia Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure, which is supported by the National Science Foundation (Grant ECCS-1542174). This work was support by the National Science Foundation Grant 1810081.

TABLE III
Parastics Extraction @ 30 GHz for Different CMIs

CMI design	R (mΩ/μm)	L (pH/μm)	G (μS/μm)	C (fF/μm)
60 μm-high CMI (AR = 2)	2.75	0.42	0.07	0.06
90 μm-high CMI (AR = 2)	2.2	0.45	0.03	0.06
90 μm-high CMI (AR = 1)	2.69	0.43	0.04	0.07

References

[1] A. Steegen, "Technology innovation in an IoT Era," in *Proc. IEEE VLSI Technol. Symp.*, Jun. 2015, pp. C170-C172.

[2] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," *IEDM Tech. Dig.*, Dec. 2011, pp. 1.1.1-1.1.6.

[3] G. Yeric, "Moore's law at 50: Are we planning for retirement?" *IEDM Tech. Dig.*, Dec. 2015, pp. 1.1.1-1.1.8.

[4] L. T. Su, S. Naffziger, and M. Papermaster, "Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade" *IEDM Tech. Dig.*, Dec. 2017, pp. 1.1.1-1.1.8.

[5] L. England and I. Arsovski, "Advanced Packaging Saves the Day! - How TSV Technology Will Enable Continued Scaling" *IEDM Tech. Dig.*, Dec. 2017, pp. 3.5.1-3.5.4.

[6] G. Hellings, *et al.*, "Active-lite interposer for 2.5 & 3D integration," in *Proc. IEEE VLSI Technol. Symp.*, Jun. 2015, pp. T222-T223.

[7] R. Mahajan, *et al.*, "Embedded multi-die interconnect bridge (EMIB) -- a high density, high bandwidth packaging interconnect," *IEEE 66th Electronic Components and Technology Conference (ECTC)*, May 2016, pp. 557-565.

[8] L. T. Su, S. Naffziger, and M. Papermaster, "Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade" *IEDM Tech. Dig.*, Dec. 2017, pp. 1.1.1-1.1.8.

[9] L. England and I. Arsovski, "Advanced Packaging Saves the Day! - How TSV Technology Will Enable Continued Scaling" *IEDM Tech. Dig.*, Dec. 2017, pp. 3.5.1-3.5.4.

[10] P. K. Jo, X. Zhang, J. L. Gonzalez, G. S. May, and M. S. Bakir, "Heterogeneous Multi-Die Stitching Enabled by Fine-Pitch and Multi-Height Compressible Microinterconnects (CMIs)," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2957-2963, July. 2018.

[11] P. K. Jo, M. Zia, J. L. Gonzalez, H. Oh, and M. S. Bakir, "Design, fabrication, and characterization of dense compressible microinterconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1003-1010, May 2017.

[12] M. O. Hossen, J. L. Gonzalez, and M. S. Bakir, "Thermomechanical Analysis and Package Level Optimization of Mechanically Flexible Interconnects (MFIs) for Interposer-on-Motherboard Assembly," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 12, pp. 2081-2089, Dec. 2018.

[13] Y. Li *et al.*, "Electromagnetic Characteristics of Multiport TSVs Using L-2L De-Embedding Method and Shielding TSVs," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 5, pp. 1541-1548, Oct. 2017.

[14] H. Yen *et al.*, "TSV RF de-embedding method and modeling for 3DIC," *SEMI Advanced Semiconductor Manufacturing Conference*, May. 2012, pp. 394-397.

[15] C. Zhang, H. S. Yang and M. S. Bakir, "Highly Elastic Gold Passivated Mechanically Flexible Interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632-1639, Oct. 2013.

[16] I. Ndip *et al*., "Analytical, Numerical-, and Measurement–Based Methods for Extracting the Electrical Parameters of Through Silicon Vias (TSVs)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 3, pp. 504-515, Mar. 2014.